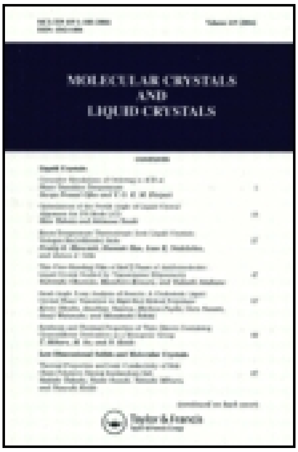

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A Study on Cu(In,Ga)Se_2 Thin-Film Characteristics During Three-Stage Process Using Real-Time Substrate Monitoring

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A Study on $Cu(In,Ga)Se_2$ Thin-Film Characteristics During Three-Stage Process Using Real-Time Substrate Monitoring

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In this study, to analyze the effect of the second stage (Cu–Se) deposition time on CIGS property, the experiment of controlling the time of the second stage was conducted. Especially, very low values were found for device properties when it was 3300s and 3500s in the second stage. It was observed that excess $Cu_{2-x}Se$ diffused excessively on the surface of the thin film, causing a lot of pores and voids on the surface. With the same evaporation ratio for each source of Cu, In, Ga, and Se, it is very important to apply the 2700s process time for the second stage in order to produce high-efficiency device. The efficiency property of device was checked through solar-simulator (AM1.5G, 100 mW/cm^2 at 25°C). In case the process time of the second stage was 2700s, efficiency was as following: 10.1%, V_{oc}: 0.53V, J_{sc}: 33.5 mA/cm^3, fill-factor: 57.2%. The analysis results obtained in this study are expected to be useful for various domestic and overseas research which aim to make high-efficiency solar cells based on proper variation of the second-stage processing time.

Keywords Cu(In; Ga)Se_2; solar cell; three-stage process; co-evaporation; temperature drop

Introduction

The key thin film of $CuInxGa_{1-x}Se_2$ (CIGS) solar cell is CIGS film which is an absorber layer. Such absorber layers can be made by various methods. However, the three-stage process method was the only one that showed a high efficiency of over 20%.[1] Also, proper supply of Cu is a very important process parameter for high efficiency. Especially, when

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Cu source is continuously supplied during the second stage, an instantaneous temperature drop occurs.[3–8] And, based on the temperature drop area, a proper composition ratio of Cu/(In+Ga) and Cu/Se can be predicted. A variety of methods are currently in research to predict such a phenomenon in order to produce high-efficiency solar cells and results of such research have been steadily published.

However, there have been only an insufficient number of research results and none of them accurately predicted the correlation between the sudden temperature drop of the substrate due to continuous supply of Cu source, growth mechanism, and efficiency. Therefore, in this study, it was researched how the process time to supply Cu-Se has effect on the Cu/(In+Ga) ratio, Cu/Se ratio, CIGS surface morphology, and the electrical property of solar-cell device. In addition, a basic research was conducted to find what happens when it is turned to the next process, the third stage, if the time of temperature drop is excessively extended.

Experiment Method

The experiment was carried out in the sequence of substrate cleaning, Mo back-contact deposition (~800 nm), CIGS absorber layer deposition (~2 μm), ZnO deposition (~800 nm) which is the window layer, and Ag-grid coating (~4 μm) as shown in Figure 1. Prior to the deposition, the substrate has been degreased in $NH_4OH+H_2O_2+H_2O$ (1:1:5) solution at 90°C for 10 min and rinsed in de-ionized water for 20 min respectively. Especially, when the CIGS absorber layer is made, the three-stage co-evaporation method[2] using the molecular beam epitaxy equipment (YAS, substrate size: 100 mm × 100 mm) was applied.

Regarding the 3-stage process, the process variables related with the time and evaporation ratio of each process are summarized in Figure 2. Concerning the Cu, In, Ga, Se source used to make the absorber layer, the product of CERAC was used. Each has 2 mm shot and granule with 99.999% purity. For the experimental results, changes in various properties were analyzed using equipment such as field emission scanning electron microscope

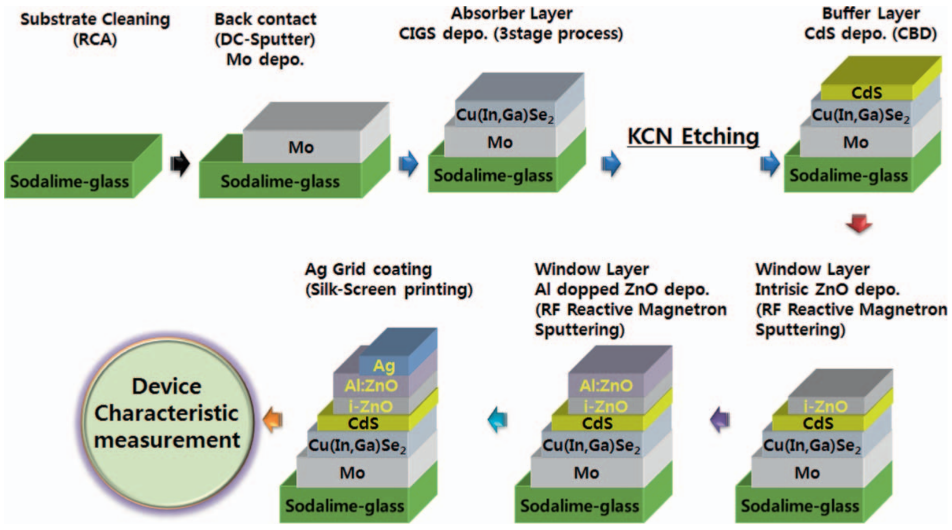

Figure 1. Device Manufacturing Processing.

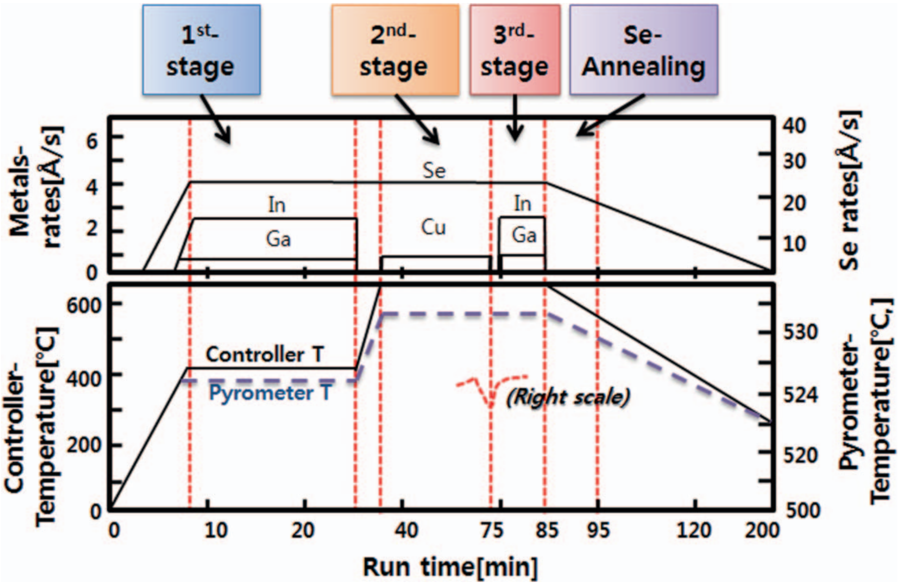

Figure 2. Experiment parameters.

(FE-SEM, S-4800, HITACHI), inductively coupled plasma atomic emission spectroscopy (ICP-AES, ICPS-8100, SHIMADZU), solar-simulator(AM1.5G, 100 mW/cm^2 at 25°C).

Also, the drop point area was investigated by measuring the substrate temperature in real time in each process. For the investigation, the pyrometer (SPT40G, WONWOO SYSTEMS) was installed at the top of the chamber to measure temperature by sensing changes in substrate emissivity.

Results and Discussion

As shown in Figure 2, this study intends to examine changes in device properties using the second-stage time as an important variable. To examine the changes, the process time was split into 2400s, 2700s, 3000s, 3300s, and 3500s, respectively. The SEM result of Figure 3 shows that the overall thickness of the thin film has no big difference. However, it was found that considerable change in the surface morphology was made as the deposition time of Cu-Se becomes longer in the second stage.

In order to provide detailed explanation on this issue, it is needed to examine the phase diagram of Figure 5 closely. In general, when Cu-Se is continuously supplied at substrate temperature of 530°C in the second stage after having deposited In, Ga and Se in the first stage, Cu ingredient generates CIGS from the surface into the $(In, Ga)_2Se_3$ phase through vacancy and converting. Cu that has been additionally supplied forms large quantity of liquid $Cu_{2-x}Se$ and small quantity of solid $Cu_{2-x}Se$, after having been diffused to the limited solid solubility. Such liquid phase $Cu_{2-x}Se$ generates CIGS thin film with large crystal grain by assisting the liquid phase sintering of small CIGS crystal grains. Newly added In and Ga in the third stage forms CIGS by consuming the liquid phase $Cu_{2-x}Se$, and forms in the direction of large grain along the grain boundary. Therefore, it enables long-range In and Ga diffusion in the direction of much larger crystal grain direction, and the empty spaces of

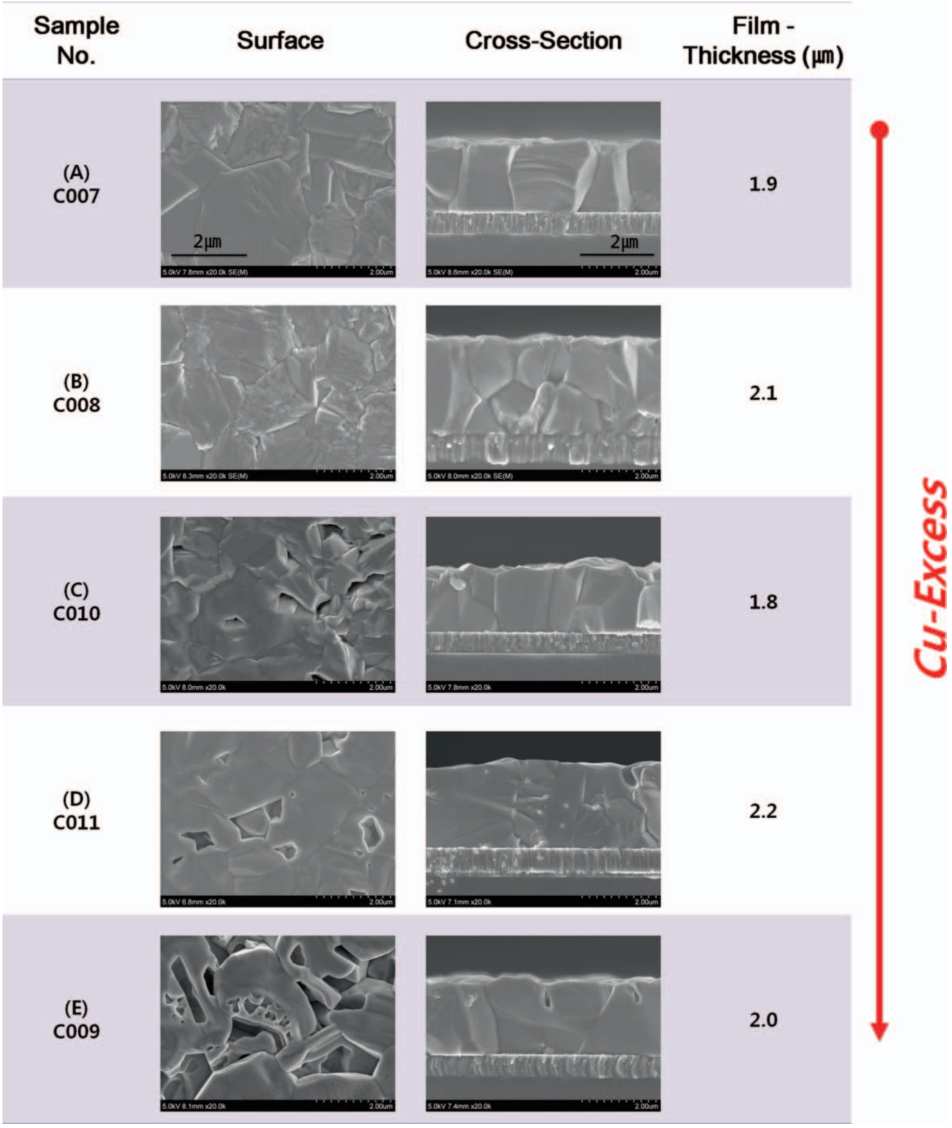

Figure 3. SEM image by different second-stage time (for Cu-Se deposition time).

the $Cu_{2-x}Se$, which has been consumed in the process, are deemed to be the pores observed on the surface of CIGS.[3,8,10]

This procedure can be easily found in the images of Figure 3(A) to (E). In this study, such growth mechanism was explained in detail in Figure 4. Particularly, the research published by Chakrabarti[8,9] shows that excessive Se deposition also plays a significant role. According to the research, when the substrate temperature is kept approximately at over 530°C, Se deposition is continuously increased. And, in the composition of Cu-Se, if Se is over 45%, all of it exists in liquified state. This was verified through experimental research (refer to Figure 5). Therefore, it was found that, to produce high-efficiency solar cells,

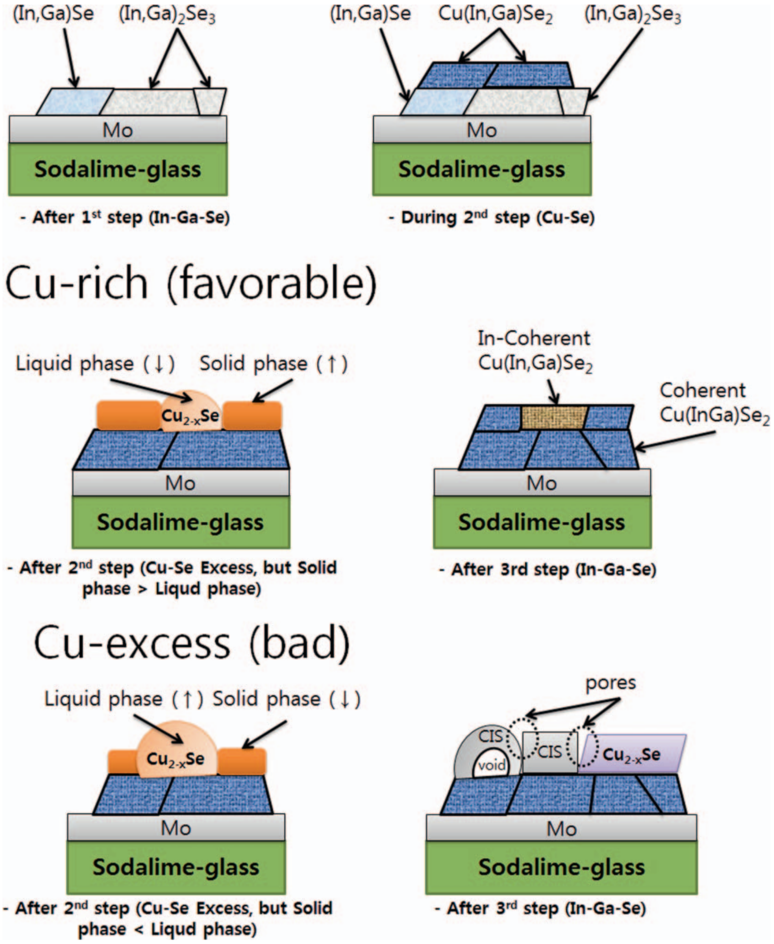

Figure 4. Cu(In,Ga)Se$_2$ Formation Mechanism under Se environment.

proper control of Cu-Se is required and that the deposition ratio and deposition time in the second stage are very important parameters if the evaporation conditions are the same.

Figure 6 shows the substrate temperature measured in real time using a pyrometer to check the temperature drop area in the second stage process. The results (values) of the measured data are shown in Table 1. Deposition time of (A) to (E) is 2400s, 2700s, 3000s, 3300s, 3500s, respectively. The dotted line shown in the figure indicates the points where the temperature drop area of each process ends. When the data of Figure 6 and Table 1 are compared overall, it is found that, as the deposition time of Cu-Se becomes longer, the width of the temperature drop area increases in proportion. The triangle-shaped points shown in Figure 6 indicate the beginning points of the third stage of (D) and (E). What is important here is that, in the temperature curves of (A) to (C), the temperature drop area begins in the second stage but the substrate temperature is recovered when the process enters the third stage.

On the other hand, in the samples of (D) and (E), temperature drop is continued. Usually, when the process is turned to the third stage, substrate temperature is recovered to the original temperature because the liquified Cu$_{2-x}$Se is exhausted due to the supply of

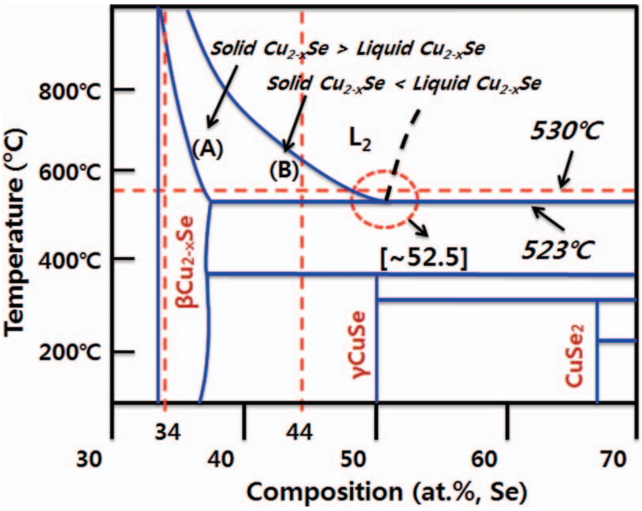

Figure 5. Phases diagram on CIGS film under low(A) and high(B) Se fluxes, respectively.

InSe, In_2Se_3 and Ga_2Se_3. However, in case $Cu_{2-x}Se$ is supplied excessively as in the cases of process time 3300s (D) and 3500s (E), the state is still the same as $Cu_{2-x}Se$(liquid) > [$Cu(In,Ga)Se_2$(solid), and $(In,Ga)_2Se_3$(solid)]. And, thus, temperature drop is continued until the end of the third stage.

Therefore, in case the 3-stage process is performed based on the deposition ratio suggested in this study, it is not reasonable to give more than 3000s for the second stage process time. Table 2 shows the ICP analysis results obtained after performing surface cleaning [by potassium cyanide (KCN)] to check the composition ratio of the thin film after the CIGS film deposition is completed. In general, when KCN etching is carried

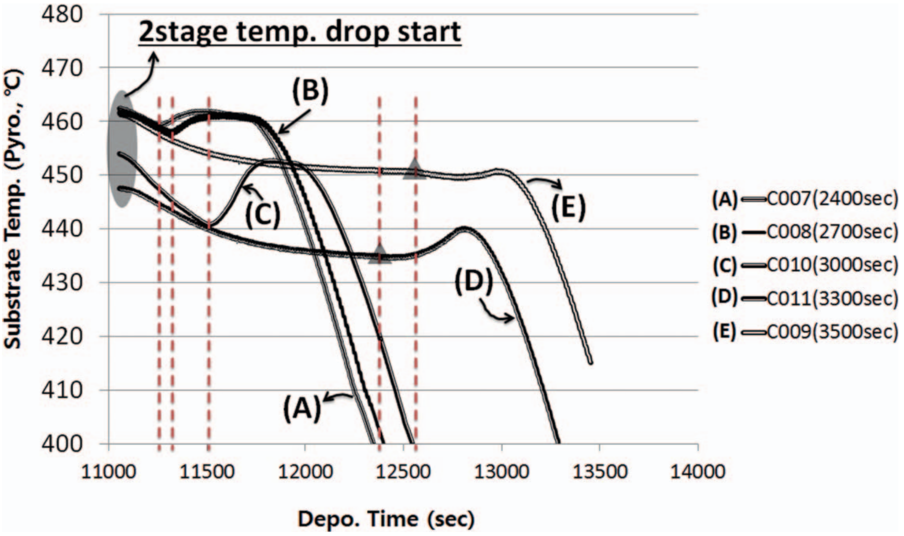

Figure 6. Temperature drop in second stage process.

Table 1. Substrate temperature drop gap in second stage process

Sample No.	Soruce Depo. Rate (Å/s)	2nd stage Process Time (sec.)	2nd stage Substrate Temp- Drop Start-Time (sec.)	Temp- Drop Gap
(A)C007	Cu: 1.0	2400	2094	463.1°C → 459.1°C drop, about 4°C drop
(B)C008	In: 4.0	2700	2586	460°C → 457.6°C drop, about 2.4°C drop
(C)C010	Ga: 0.7	3000	1660	454.5°C → 440.8°C drop, about 13.7°C drop
(D)C011	Se: 15∼18	3000	2014	447.6°C → 434.8°C drop, about 12.8°C drop
(E)C009		3300	1934	461.8°C → 450.5°C drop, about 11.3°C drop

out, solution made up of 70 ml of de-ionized water and 0.5 g of KCN powder at room temperature is used, and the substrate on which CIGS absorption layer has been deposited is dipped in this KCN diluted solution for 1 minute.

KCN treatment is carried out to remove impurities on the surface and the secondary phase such as $Cu_{2-x}Se$ that deteriorates efficiency of device composition.[11,12,13] According to ICP analysis results, as the process time of the second stage becomes longer, the Cu/(In+Ga) ratio gradually increases. However, in the case of (C) C010 where the process time was 3000s, it was found that the Cu/(In+Ga) ratio abruptly dropped. In case Cu-Se is deposited immediately after the first stage, the CIGS which is in poor state leads to Cu diffusion to (In, Ga)-Se due to the continuous Cu-Se deposition. Through the process, if the liquified $Cu_{2-x}Se$ phase locally existing on the surface of the thin film is mixed excessively, diffusion occurs

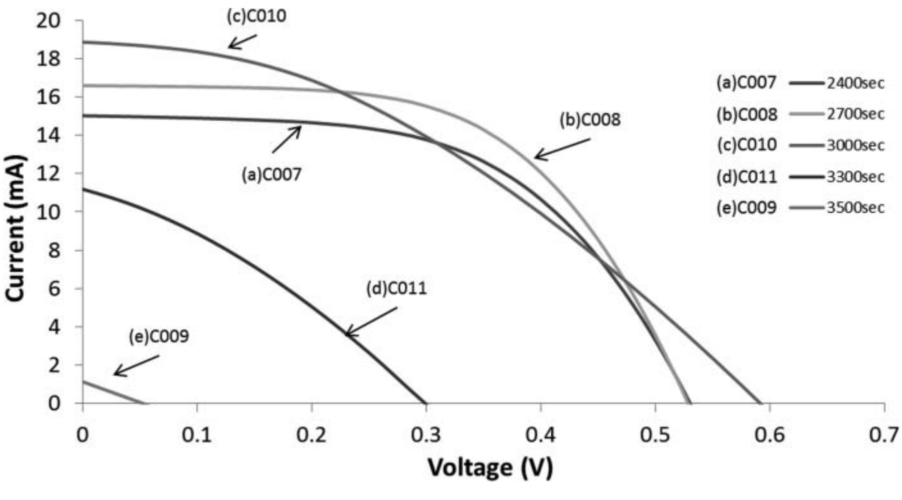

Figure 7. The various I–V curves of CIGS thin-film solar cell fabricated with different second stage time (aperture area: 0.495 cm^2).

Table 2. ICP measurement results

Sample No.	2nd-stage process Time (sec.)	Mol Fraction (%)				Composition-ratio			
		Cu	In	Ga	Se	Cu/ (In+Ga)	Ga/ (In+Ga)	Cu/Se Cu/Se	(In+Ga)/ Se
(A)C007	2400	19.16	18.38	6.81	55.64	0.76	0.27	0.34	0.45
(B)C008	2700	20.28	15.69	9.44	54.59	0.81	0.38	0.37	0.46
(C)C010	3000	17.53	20.31	6.95	55.21	0.64	0.25	0.32	0.49
(D)C011	3300	23.20	17.78	6.72	52.31	0.95	0.27	0.44	0.47
(E)C009	3500	23.33	16.87	7.27	52.53	0.97	0.30	0.44	0.46

in the whole surface. Regarding liquid phase over a proper level, after completion of CIGS film deposition, when the substrate is cooled, the liquid secondary phase is changed to solid phase and is separated from CIGS phase. This means that adhesion is not good compared to other samples. That is, a large amount of $Cu_{2-x}Se$ phase that existed on the surface was removed considerably due to KCN etching. And, that is why a lower composition ratio of Cu/(In+Ga) was observed compared to other samples (about Cu/(In+Ga) = ~0.85).

Table 3 shows the parameter of the solar cell made through the experiment. As the time of the second stage increased, the short circuit current (J_{sc}), open circuit voltage (V_{oc}) and fill factor increased and then decreased. Especially, when ICP was measured, it was found that the electric current and open circuit voltage of the (D) and (E) samples with a Cu/(In+Ga) ratio of over 0.95 sharply decrease. When the SEM image (Figure 3) with the Cu content of over 0.95 is reviewed, one can find the huge void made on the surface of the thin film. The void was made because $Cu_{2-x}Se$ was removed due to KCN etching. The diameter of the huge void is approximately over 200 nm and that makes the rough surface. In general, $Cu_{2-x}Se$ has semi-metallic property and also has high electric charge concentration of over 10^{21} cm^3.[14] In case the CdS, about 50–80 nm thick, is deposited on the CIGS surface, the big voids may not be completely covered. It rather functions as a leakage path, deteriorating the junction property of the solar cell.[15] Therefore, it is judged that this is the reason why the open circuit voltage, fill-factor, and efficiency, all of them dropped sharply as shown in the measuring results of Table 3 (D) and (E).

Also, sample (c) show relatively high efficiency (Table 3), even at very low Cu/(In+Ga) composition. In the case of sample (c), substantial quantity of $Cu_{2-x}Se$ did not appear to react with In and Ga, but, rather, remained on the surface during the second stage process.

Table 3. Cell parameters of CIGS solar cells as a time of second stage

Sample No.	Area(cm^2)	V_{oc}(V)	J_{sc} (mA/cm^2)	F.F.(%)	Eff. (%)
(A)C007	0.495	0.437	30.17	38.74	5.11
(B)C008	0.495	0.53	33.51	57.2	10.1
(C)C010	0.495	0.57	38.34	42.28	9.22
(D)C011	0.495	0.30	22.59	31.99	2.16
(E)C009	0.495	0.053	2.3	5.32	0.006

It is deemed that the ratio of Cu/(In+Ga) is relatively low due to loss of large quantity of these due to KCN etching.

However, although the composition on the bulk side following KCN etching is low, the status of surface roughness is good and, in particular, sample (c) has substantially better status of grain growth in comparison to other samples when the cross-section under SEM is compared. Accordingly, it is forecasted that movement of electric charges generated near the CdS/CIGS interface would be easy and recombination within the bulk will be lower at the time of fabrication of final solar cell. It is, therefore, deemed that this will result in improved electrical properties, thereby achieving better efficiency compared to other samples.

In addition, the fact that composition of Cu is relatively low signifies that Cu(In,Ga)$_3$Se$_5$ phase, which is a n-type Cu-poor phase, could have been formed throughout the entire surface of thin film after etching, and this also signifies that there is possibility of improvement of electrical property by converting CIGS thin film, which is heterojunction, into homojunction.

Conclusions

In this study, to analyze the effect of Cu-Se deposition time on CIGS property, the experiment of controlling the time of the second stage was conducted. The thin film was deposited with the same evaporation amount for each source and the experiment was carried out with the process time for the second stage, split into 2400s, 2700s, 3000s, 3300s, and 3500s, respectively. The best result was obtained when it was 2700s. Especially, very low values were found for device properties when it was 3300s and 3500s in the second stage. It was observed that excess Cu$_{2\text{-x}}$Se diffused excessively on the surface of the thin film, causing a lot of pores and voids on the surface. What grabs attention here is that, in the temperature curves of 2400s to 3000s, the temperature drop area of the second stage begins and when it is turned to the third stage, substrate temperature is recovered. On the other hand, in the samples of 3300s and 3500s, temperature drop is continued. That is, in case Cu$_{2\text{-x}}$Se is supplied excessively during process time, even after it is turned to the third stage, it is still in the state of Cu$_{2\text{-x}}$Se (liquid) $>$ [Cu(In,Ga)Se$_2$(solid), and (In,Ga)$_2$Se$_3$(solid)] and thus temperature drop is continued until the end of stage 3. Through such process, the behavior of thin film growth of the Cu-excess CIGS absorber layer in the second stage can be explained. Therefore, if the 3-stage process is performed based on the evaporation ratio suggested in this study, it is not reasonable to give more than 3000s in the second stage. With the same evaporation ratio for each source of Cu, In, Ga, and Se, it is very important to apply the 2700s process time for the second stage in order to produce high-efficiency device.

The efficiency property of device was checked through solar-simulator (AM1.5G, 100 mW/cm^2 at 25°C). In case the process time of the second stage was 2700s, efficiency was as following: 10.1%, V$_{oc}$: 0.53V, J$_{sc}$: 33.5 mA/cm^2, fill-factor: 57.2%.

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